CMT10XXX Isolated CAN Transceiver

1 Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL 1577 component recognition program
  - CSA component notice 5A
  - CQC approval per GB4943.1-2022
  - Fully compatible with the ISO11898-2 standard
- Up to 5 kV_{RMS} insulation voltage
- Power supply voltage
  - VDD1 : 2.5V to 5.5V
  - VDD2 : 4.5V to 5.5V
- Data rate: 1Mbps (CMT1050)
  5Mbps (CMT1042/CMT1052)
- Bus fault protection of -70V to +70V
- Common-Mode Voltage Range: ±30 V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Ideal Passive, High Impedance Bus and Logic Terminals When Unpowered
- High CMTI: 150kV/us
- HBM ESD tolerance on bus pins: 6 kV
- Operation temperature: -40°C to 125°C
- Low loop delay: ＜220 ns
- High system level EMC performance: Enhanced system level ESD, EFT, Surge immunity
- (WB) SOIC16 and SOW8L package

2 Applications

- Isolated CAN Bus
- AC and servo drives
- Solar inverters
- PLC and DCS communication modules
- Battery charging and management
- Elevators and escalators
- Industrial power supplies

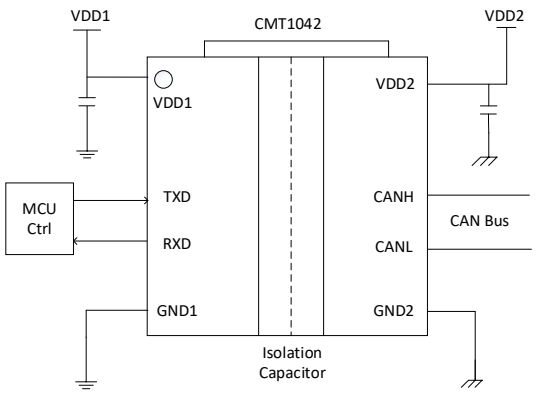
3 Description

The CMT10XXX is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The CMT10XXX integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on CMOSTEK capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The CMT10XXX device is safety certified by UL1577 and supports 5 kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions. The data rate of the CMT10XXX is up to 5 Mbps. The CMT10XXX provides thermal protection and transmit data dominant time out function.

Device Information

器件型号	封装	封装尺寸（标称值）（mm）
CMT1050	SOW8L	5.85 * 7.50
CMT1042		5.85 * 7.50
CMT1050W	SOIC16-WB	10.30 * 7.50
CMT1052W		10.30 * 7.50
CMT1042W		10.30 * 7.50

Simplified Schematic



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4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage[2]	VDD1, VDD2		-0.5	6.5	V
Maximum input voltage	V_{IN}		-0.4	VDD+0.4	V
Maximum BUS pin voltage	V_{CANH}, V_{CANL}		-70	+70	V
Output current	I_O		-15	15	mA
Operating Temperature	Topr		-40	125	℃
Storage temperature	T_{STG}		-65	150	℃
Electrostatic discharge	HBM			±6000	V
	CDM			±2000	V

Notes:

[1]. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

[2]. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
Supply voltage, controller side	VDD_1	2.5		5.5	V	
Supply voltage, bus side	VDD_2	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-30		30	V	
High level input voltage	V_{IH}	0.7*VDD1		5.5	V	TXD
Low level input voltage	V_{IL}	0		0.3*VDD1	V	TXD
High level output current	I_{OH}	-70			mA	Driver
		-6				Receiver
Low level output current	I_{OL}		70	70	mA	Driver
			6	6		Receiver
Operating temperature	T_A	-40		125	℃	
Junction temperature	T_J	-40		150	℃	

6 Thermal Information

Table 3. Thermal Information

Parameters	Symbol	SOW8L	（WB）SOIC16	Unit
Junction-to-ambient thermal resistance	θ_{JA}	100	69.9	℃/W
Junction-to-board thermal resistance	θ_{JB}	51.8	29	
Junction-to-case（top）thermal resistance	$\theta_{JC(top)}$	40.8	31.8	

7 Pin Description

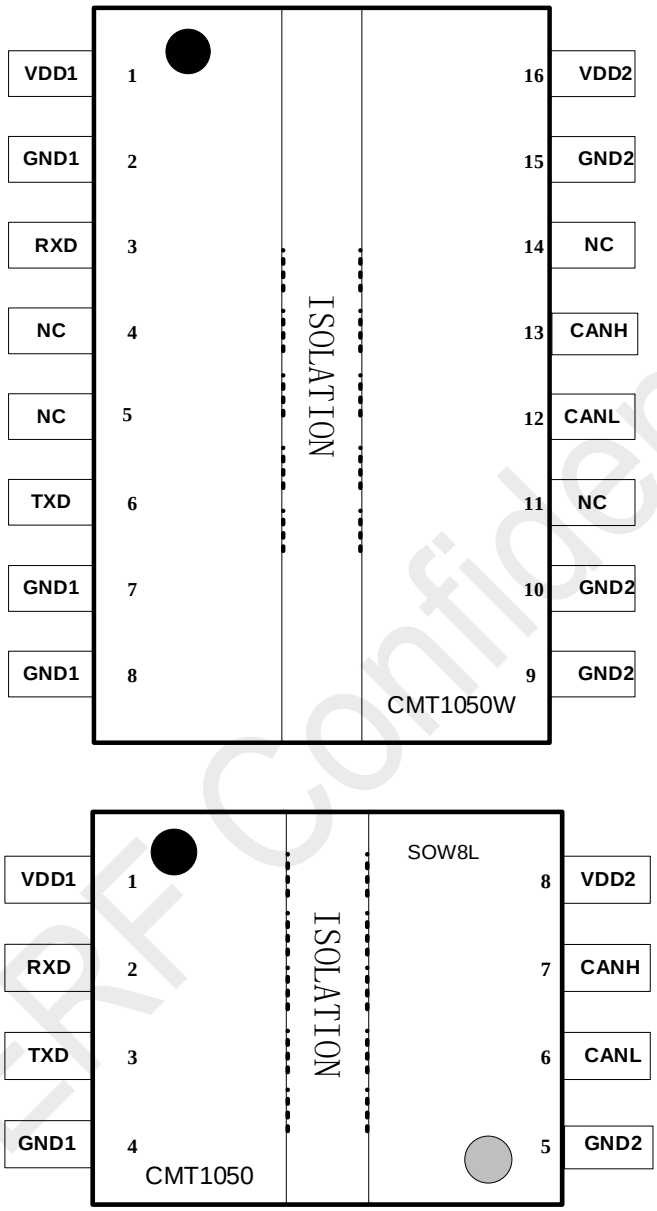


Figure 1. CMT1050X Pin Configuration

Table 4. CMT1050X Pin Description

Pin Name	Pin number		Description
	CMT1050W	CMT1050	
VDD1	1	1	Power supply for isolator side 1
RXD	3	2	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
TXD	6	3	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND1	2,7,8	4	Ground reference for Isolator Side 1

Pin Name	Pin number		Description
GND2	9,10,15	5	Ground reference for Isolator Bus Side
CANH	13	7	High-level CAN bus line
CANL	12	6	Low-level CAN bus line
VDD2	16	8	Power supply for isolator side 2.
NC	4,5,11,14		No Connection

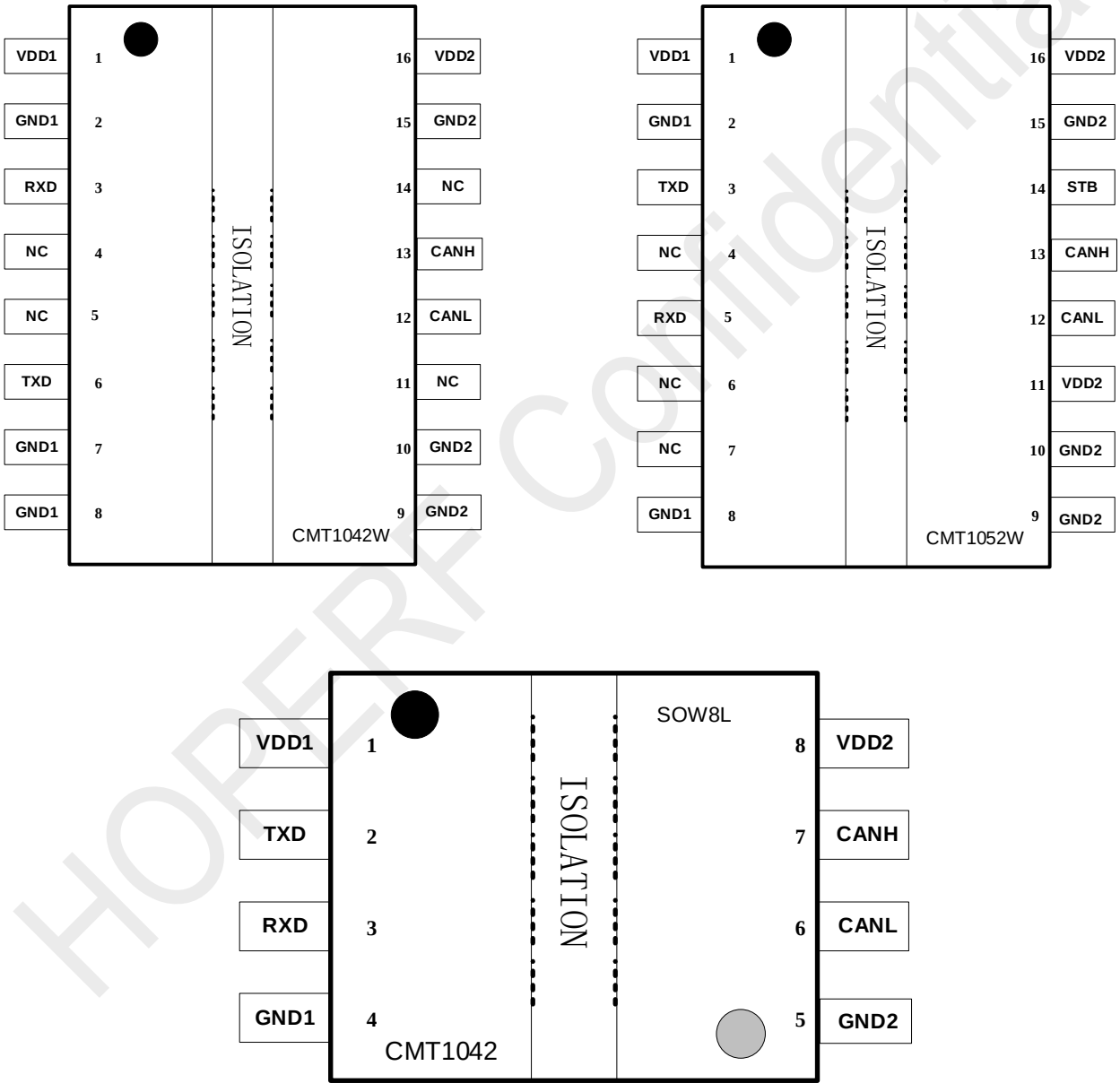


Figure 2. CMT1042W and CMT1052W /CMT1042 Pin Configuration

Table 5. CMT1052X/CMT1042X Pin Description

Pin Name	Pin number			Description
	CMT1052W	CMT1042W	CMT1042	
VDD1	1	1	1	Power supply for isolator side 1
TXD	3	3	2	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
RXD	5	5	3	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
GND1	2,8	2,8	4	Ground reference for Isolator Side 1
GND2	9,10,15	9,10,15	5	Ground reference for Isolator Bus Side
CANH	13	13	7	High-level CAN bus line
CANL	12	12	6	Low-level CAN bus line
VDD2	11,16	11,16	8	Power supply for Bus Side, PIN11 must be connected externally to PIN16
NC	4,6,7	4,6,7,14		No Connection
STB	14			Standby mode control input

8 Typical Application

8.1 Typical Application Schematic

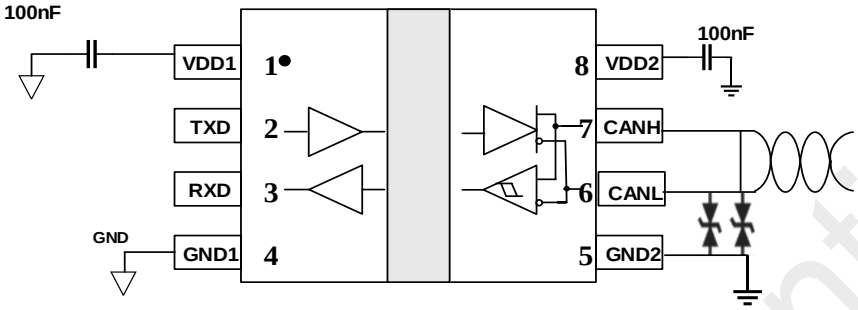


Figure 3. Typical Application Schematic

Note: *users should be careful not to connect ground and VDD reversely.*

8.2 PCB Layout Guidelines

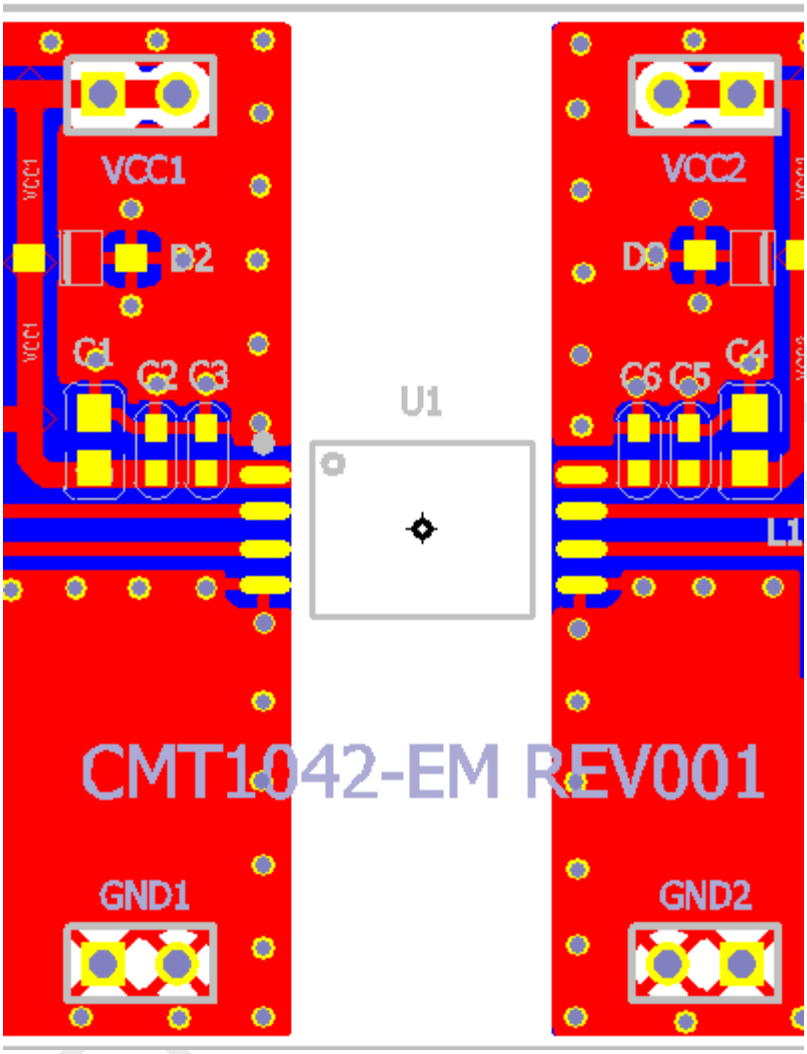


Figure 4. Recommended PCB Layout (Top layer)

9 Parameter Measurement Circuit Setup

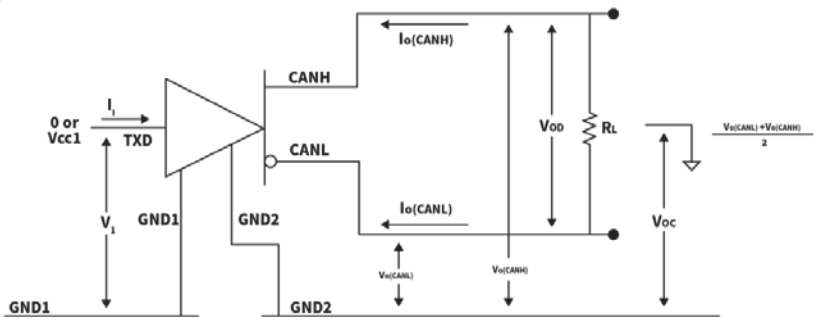


Figure 5. Driver Voltage, Current and Test Definition

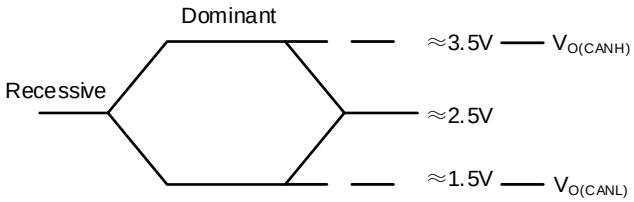


Figure 6. Bus Logic State Voltage Definitions

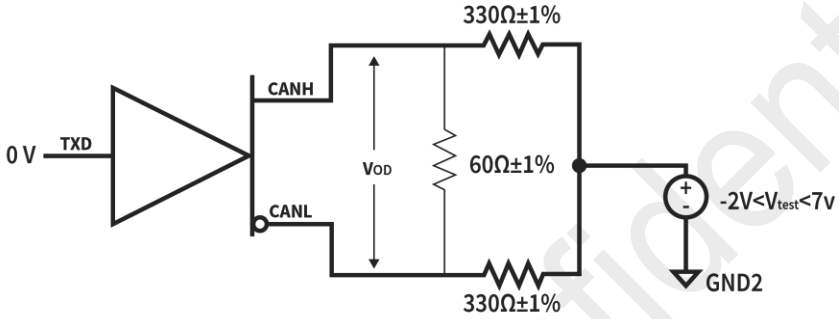
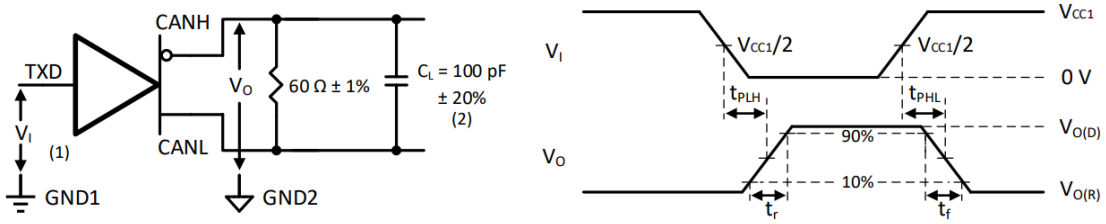


Figure 7. Driver VOD with Common-mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6 ns, t_f≤ 6ns, Zo = 50Ω

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 8. Driver Test Circuit and Voltage Waveform

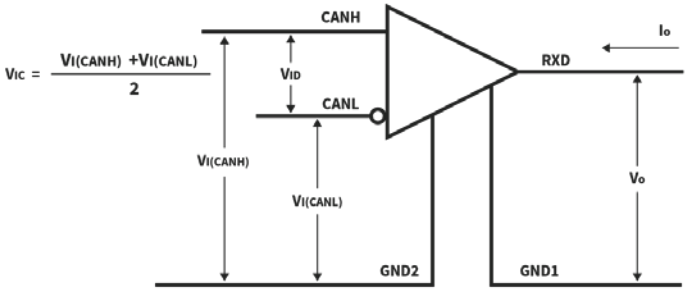
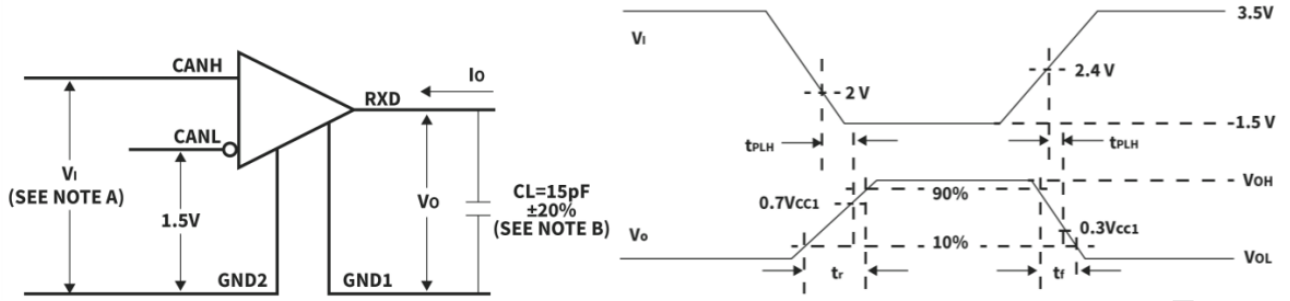


Figure 9. Receiver Voltage and Current Definition



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6 ns, t_f≤ 6ns, Zo = 50Ω

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 10. Receiver Test Circuit and Voltage Waveform

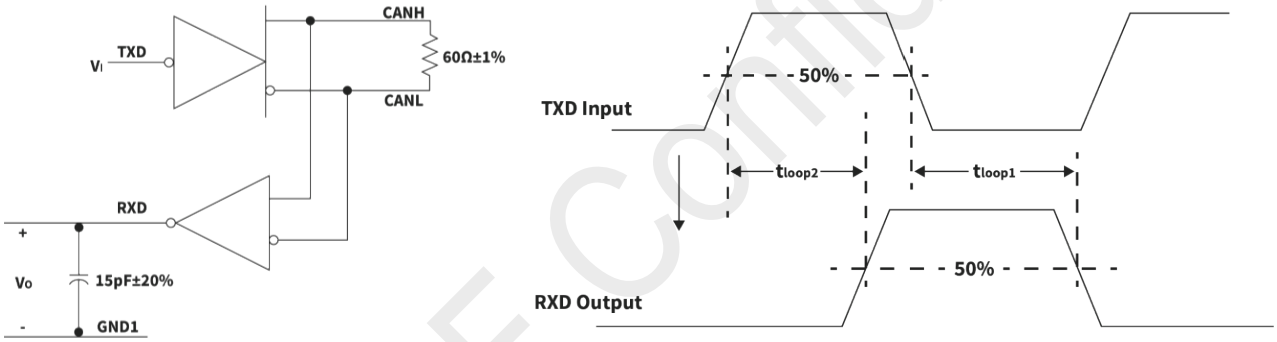
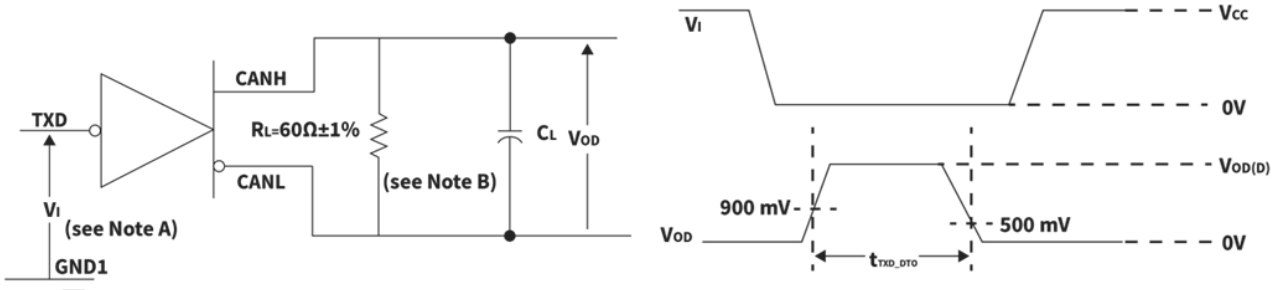


Figure 11. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6 ns, t_f≤ 6ns, Zo = 50Ω

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 12. Dominant Time-out Test Circuit and Voltage Waveform

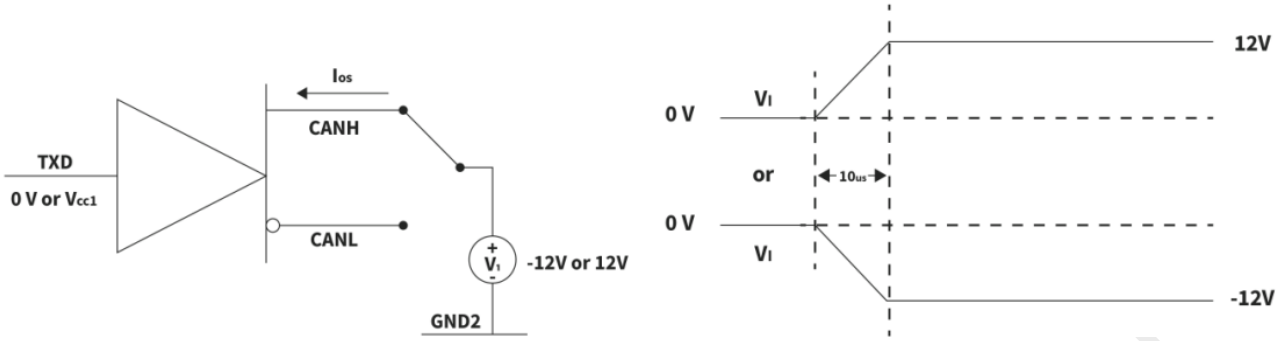


Figure 13. Driver Short-Circuit Current Test Circuit and Waveform

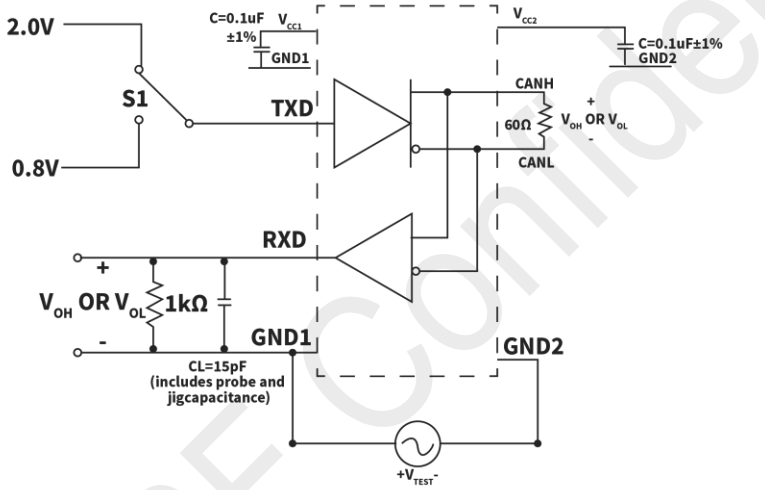


Figure 14. Common-Mode Transient Immunity Test Circuit

10 Electrical Specifications

10.1 Electrical Characteristics

VDD1 = 2.5V ~ 5V, VDD2 = 4.5V~5.5V, T_A= -40 to 125 ℃. Unless otherwise noted, Typical values are at VDD1= 3.3V，VDD2 = 5V，T_A = 25℃）

Table 6. Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD1		2.5		5.5	V
	VDD2		4.5	5	5.5	V
Logic side supply current	IDD1	VDD_1 = 3.3 V, TXD = 0		2.2	3.50	mA
		VDD_1 = 3.3 V, TXD = VDD1		1.1	2.00	
		VDD_1 = 5 V, TXD = 0		2.2	3.50	mA
		VDD_1 = 5 V, TXD = VDD1		1.1	2.00	

Bus side supply current	IDD2	VI = 0V, R_{load} = 60Ω		46	70	mA
		VI = VDD_2		5.3	10	
Thermal-shutdown Threshold	T_{TS}		155	165	180	℃
Common Mode Transient Immunity	CMTI		±100	±150		kV/us
Logic Side						
High level input voltage	V_{IH}	TXD pin	0.7*V_{DD1}			V
Low level input voltage	V_{IL}	TXD pin			0.3*V_{DD1}	V
High level input current	I_{IH}	TXD pin		0		uA
Low level input current	I_{IL}	TXD pin	-15			uA
High level output voltage	V_{OH}	I_{OH} =-4mA, RXD pin	V_{DD1}- 0.4			V
Low level output voltage	V_{OL}	I_{OL} = 4mA, RXD pin			0.4	V
Input Capacitance	C_{IN}	TXD pin		6.5		pF
Driver						
CANH output voltage (Dominant)	V_{OH}	TXD=0 V, R_{LOAD}= 60Ω	2.8	3.4	4.5	V
CANL output voltage (Dominant)	$V_{OL(D)}$	TXD=0 V, R_{LOAD}= 60Ω	0.8	1.2	2.25	V
CAN bus output voltage (Recessive)	$V_{O(R)}$	TXD=VDD1, R_{LOAD}= 60Ω	2	0.5*V_{DD2}	3	V
Differential output voltage (Dominant)	$V_{OD(D)}$	VDD=5V, TXD=0, R_{load} = 60Ω	1.5		3	V
Differential output voltage (Recessive)	$V_{OD(R)}$	VDD=5V, TXD=V_{IO}, R_{load}= 60Ω	-0.05		0.05	V
		VDD=5V, TXD=V_{IO}, No load.	-0.1		0.1	
Dominant short-circuit output current	$I_{O(SC)DOM}$	TXD=0V, t＜$t_{to(dom)TXD}$. V_{CANH}= -30V	-100		-40	mA
		TXD=0V, t＜$t_{to(dom)TXD}$. V_{CANL}=30V	40		100	
Recessive short-circuit output current	$I_{O(SC)REC}$	Normal/Silent mode; Vtxd=VDD1; V_{CANH}= V_{CANL}=-27V to +30V	-6		6	mA
Receiver						
Positive-going bus input threshold voltage	V_{IT+}			750	900	mV
Negative-going bus input threshold voltage	V_{IT-}		500	650		mV
Hysteresis voltage	V_{HYS}			100		mV
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	V_{CANH}= V_{CANL}=5V, VDD=0V, VIO=0V	-5		5	uA
Input capacitance to ground	C_I	CANH or CANL		13		pF
Differential input	C_{ID}			5		pF
Differential input resistance	R_{ID}		20		40	kΩ
Input resistance	R_{IN}		15	30	40	kΩ
Input resistance matching	RI_{MATCH}	CANH = CANL	-5		+5	%
Common-mode voltage range	V_{COM}		-30		+30	V

10.2 Switching Electrical Characteristics

VDD1 = 2.5V ~ 5V, VDD2 = 4.5V~5.5V, T_A= -40 to 125 ℃. Unless otherwise noted, Typical values are at VDD1= 3.3V，VDD2 = 5V，T_A = 25℃）

Table 7. Switching Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Loop delay1	T_{LOOP1}	Driver input to receiver output, Recessive to Dominant		120	220	ns
Loop delay2	T_{LOOP2}	Driver input to receiver output, Dominant to Recessive		100	220	ns
Transmitted recessive bit width	$T_{bit(bus)}$	$T_{bit(TXD)}$= 500ns	435	488	530	ns
		$T_{bit(TXD)}$= 200ns	155	186	210	
Bit time on RXD pin	$T_{bit(RXD)}$	$T_{bit(TXD)}$= 500ns	400	490	550	ns
		$T_{bit(TXD)}$= 200ns	150	191	240	
Driver						
Propagation delay time, recessive -to- dominant output	t_{PLH}			73		ns
Propagation delay time, dominant-to-recessive output	t_{PHL}			63		ns
Differential output signal rise time	t_r			62		ns
Differential output signal fall time	t_f			60		ns
Bus dominant time-out time	t_{TXD_DTO}		800	1900	4000	us
Receiver						
Propagation delay time, low to high level output	t_{PLH}			58		ns
Propagation delay time, high to low level output	t_{PHL}			46		ns
RXD signal rise time	t_r			1		ns
RXD signal fall time	t_r			1		ns

10.3 Insulation Specifications

Table 8. Insulation and Safety Related Specifications

Description	Sym	Condition	Value		Unit
			SOW8L	WB SOIC-16	
Min. External clearance[1](air gap)	CLR	The shortest terminal-to-terminal distance through air	8.0	8.0	mm
External creepage[1] (tracking)	CRP	The shortest terminal-to-terminal distance across the package surface	8.0	8.0	mm
Distance through insulation	DTI	Minimum internal gap	18		um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11);	>600		V
Material group	-	IEC 60112	I		-
Installation Classification per DIN VDE 0110	-	Rated mains voltage ≤ 150 V_{RMS}	I to IV	I to IV	-
		Rated mains voltage ≤ 300 V_{RMS}	I to IV	I to IV	-
		Rated mains voltage ≤ 600 V_{RMS}	I to IV	I to IV	-
		Rated mains voltage≤ 1000 V_{RMS}	I to III	I toIII	
Installation Classification perDIN VDE V 0884-11:2017-01[2]					
Climatic Category			40/125/21		
Pollution Degree		Per DIN VDE 0110	2		
Maximum repetitive isolation voltage	V_{IORM}		1414		V_{pk}
Maximum isolation working voltage	V_{IOWM}	AC voltage (sine wave); Time dependent dielectric breakdown	1000		V_{RMS}
		DC voltage	1414		V_{DC}
Input to output test voltage, method B1	$V_{pd(m)}$	$V_{ini.b}$= V_{iotm}, $V_{pd(m)}$= V_{iorm}*1.875, t_{ini}= t_m = 1 sec,	＜5		pc
Input to output test voltage, method A. After environmental tests subgroup 1	$V_{pd(m)}$	$V_{ini.a}$= V_{iotm}, $V_{pd(m)}$= V_{iorm}*1.6, t_{ini}= 60 sec, t_m = 10 sec,	＜5		pc
Input to output test voltage, method A. After input and output safety test subgroup 2 and subgroup 3	$V_{pd(m)}$	$V_{ini.a}$= V_{iotm}, $V_{pd(m)}$= V_{iorm}*1.2, t_{ini}= 60 sec, t_m = 10 sec,	＜5		pc
Maximum transient isolation voltage	V_{IOTM}	t = 60 s (qualification);	7000		V_{pk}
Maximum surge isolation voltage[3]	V_{IOSM}	Test method per IEC62368-1, 1.2/50 us waveform, V_{TEST} = 1.6 x V_{IOSM}	6250		V_{pk}
Isolation capacitance, input to output[5]	C_{IO}	f = 1 MHz	1.2		pF
Isolation resistance, input to output[5]	R_{IO}	V_{IO} = 500 V, T_{amb} = T_s	$>10^9$		Ω
		V_{IO} = 500 V, 100℃≤T_{amb}≤125℃	$>10^{11}$		
UL 1577					
Withstand isolation voltage	V_{ISO}	V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	5000		V_{RMS}

Notes:

[1]. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

[2]. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

[3]. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

[4]. Apparent charge is electrical discharge caused by a partial discharge (pd).

[5]. All pins on each side of the barrier are tied together creating a two-terminal device.

10.4 Safety-related Certifications

Table 9. Safety-related Certifications

VDE	UL		CQC	TUV
DIN VDE V0884-11:2017-01	UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	GB 4943.1-2022	EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2: 2013
Certificate number: pending	Certificate number: E541580		Certificate number: CQC23001382478	Certificate number: pending

10.5 Safety Limiting Values

Reinfored isolation safety-limiting values as outlined in VDE-0884-11 of CMT10XXX

Table 10. Safety Limiting Values

Parameters	Test Condition	Value	Unit
Safety supply power	$R_{\theta JA}$ = 100 °C/W, T_J = 150°C, T_A = 25 °C	1250	mW
			mA
Safety supply current	$R_{\theta JA}$ = 100 °C/W, V_I = 5 V, T_J = 150 °C, T_A = 25 °C	250	W
Satefy temperature		150	℃

1. Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 （300mil）package which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2. The maximum safety temperature has the same value as the maximum junction temperature(T_j)specified for the device.

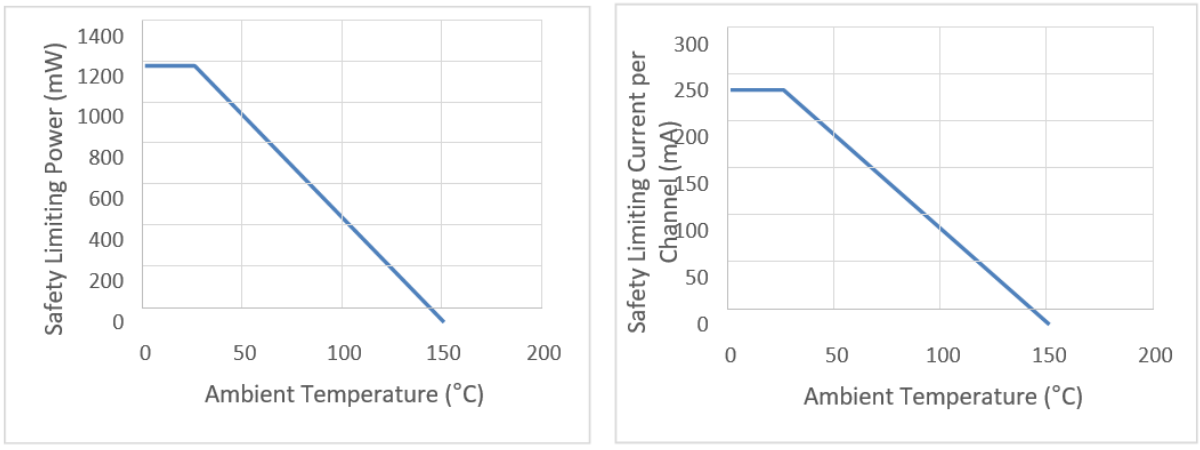


Figure 15. CMT10XXX Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

11 Function Description

11.1 Function Overview

The CMT10XXX is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The CMT10XXX integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on CMOSTEK capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The CMT10XXX device is safty certified by UL1577 support 5 kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the CMT10XXX is up to 5Mbps. The CMT10XXX provides thermal protection and transmit data dominant time out function.

11.2 Functional Modes

The table below lists the functional modes of the CMT10XXX.

Table 11. Driver Function Table

TXD	CANH	CANL	BUS STATE
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive
Notes: H = high level; L = low level; Z = common mode (recessive) bias to VDD/2			

Table 12. Receiver Function Table

V_{ID} = CANH-CANL	RXD	BUS STATE
$V_{ID} \geqslant 0.9V$	L	Dominant
$0.5 < V_{ID} < 0.9V$	X	Uncertain
$V_{ID} \leqslant 0.5V$	H	Recessive
Open	H	Recessive
Notes: H = high level; L=low level; X=uncertain		

11.3 Standby mode

The CMT10XXX cannot transmit or receive regular CAN messages in Standby mode. Only the isolator and low-power CAN receiver are active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{filtr(wake)bus}$ are reflected on the RXD pin. To reduce current consumption, the CAN bus is terminated to GND and not biased to VDD2/2 as in Normal mode. Standby mode is selected by setting pin STB HIGH. An internal pull-up ensures that Standby mode is selected by default when pin STB is not connected.

In Standby mode;

- The CAN transmitter is off
- The normal CAN receiver is off
- The low-power CAN receiver is active
- CANH and CANL are biased to GND

- The signal received at the low-power CAN receiver is reflected on pin RXD

The isolation function of the CMT10XXX is not disabled in Standby mode. Overall quiescent current is not reduced significantly in this mode. The CMT10XXX is not designated to support CAN bus wake-up functionality with very low quiescent currents.

11.4 Bus Dominant Time-out Function

In standby mode, a “bus dominant time-out” timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is forced HIGH

11.5 TXD Dominant Time-out Function

A TXD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (T_{txd_dto}), the transmitter is disabled, drving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

11.6 Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

11.7 Over Temperature Protection

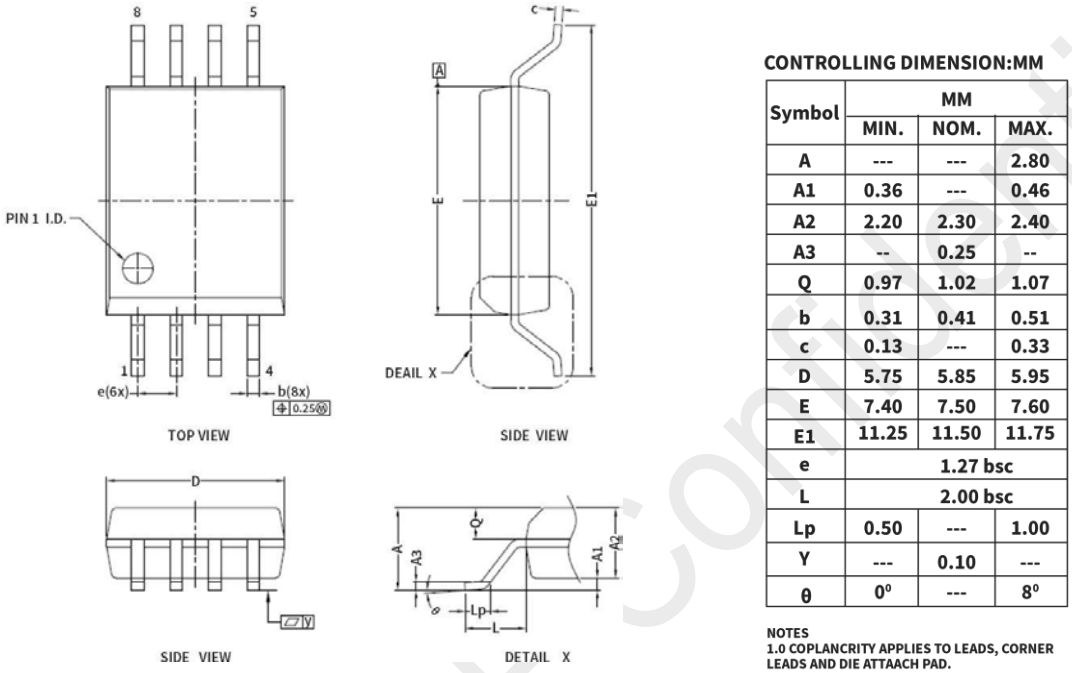
The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{ts}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{ts} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

12 Packaging Information

The packaging information of the CMT10XXX is shown in the figures below.

12.1 CMT10XXX SOW8L Packaging



CONTROLLING DIMENSION:MM

Symbol	MM		
	MIN.	NOM.	MAX.
A	---	---	2.80
A1	0.36	---	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	---	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	---	1.00
Y	---	0.10	---
θ	0°	---	8°

NOTES
1.0 COPLANCRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTAACH PAD.

Figure 16. CMT10XXX SOW8L Packaging

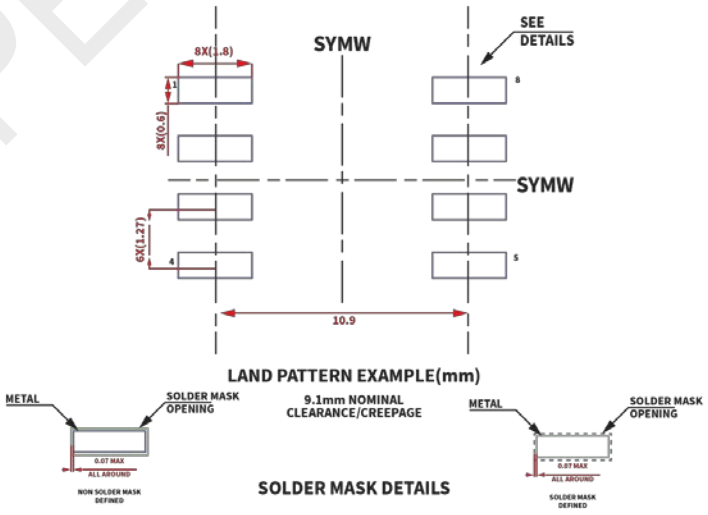
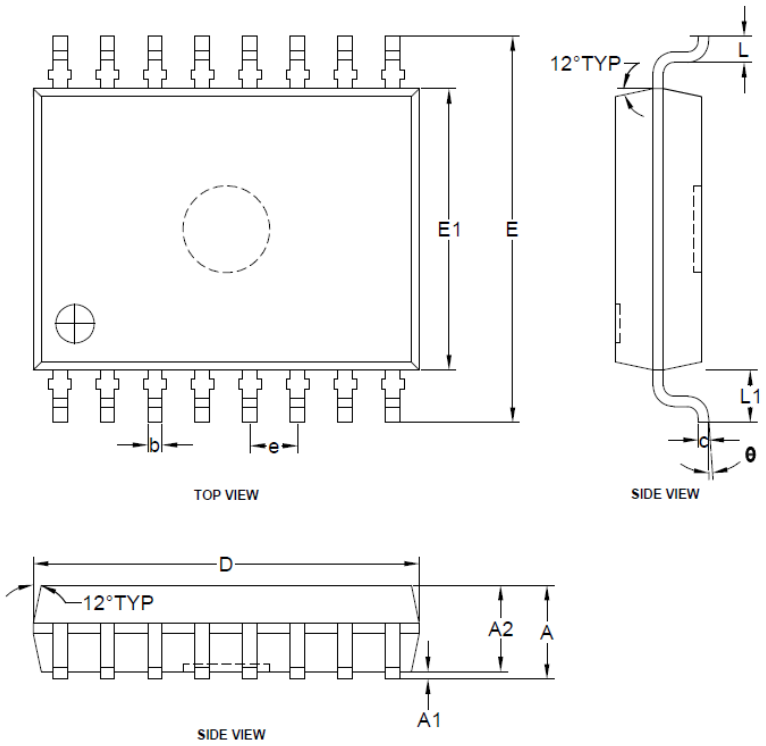


Figure 17. CMT10XXX SOW8L Package Board Layout Example

12.2 CMT10XXX SOIC16 Packaging



Symbol	Size (mm)		
	Min	TYP	Max
A	--	--	2.700
A1	0.100	0.200	0.300
A2	2.200	2.300	2.400
b	0.350	0.400	0.450
c	0.100	0.205	0.300
D	10.100	10.300	10.500
E	10.100	10.400	10.700
E1	7.300	7.500	7.700
e	1.270BSC		
L	0.550	0.700	0.850
L1	1.400BSC		
θ	0°	4°	8°

Figure 18. CMT10XXX SOIC 16 Package Shape and Dimension in Millimeter

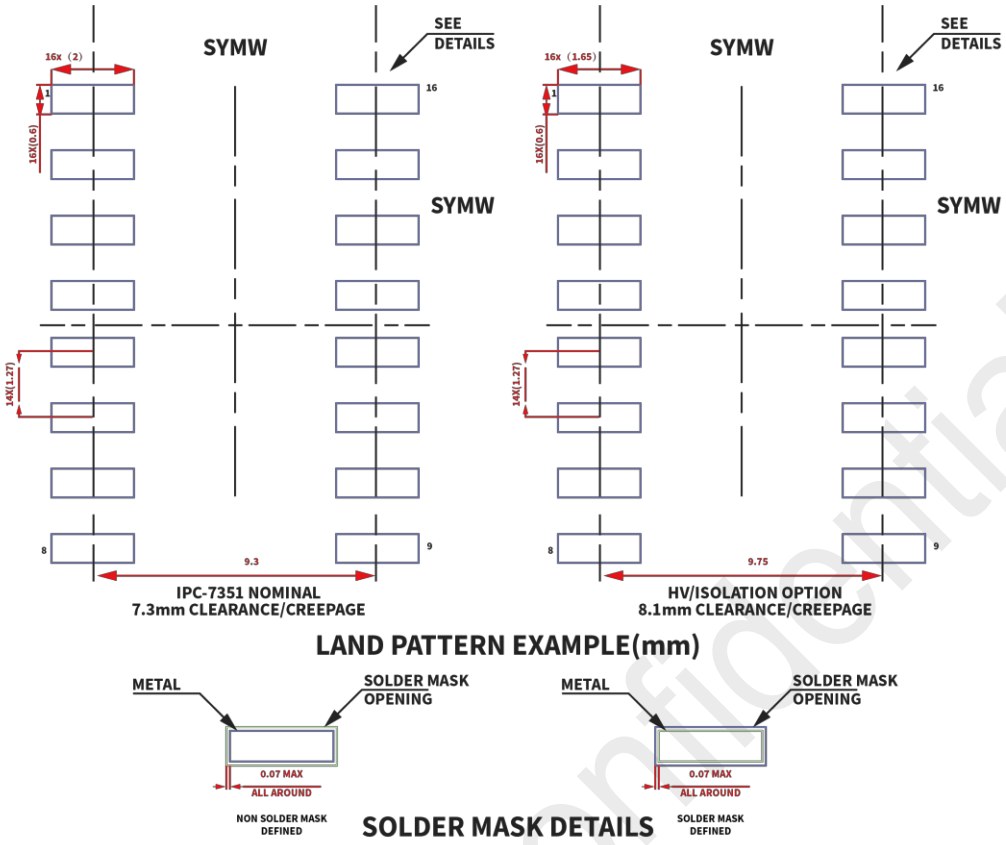


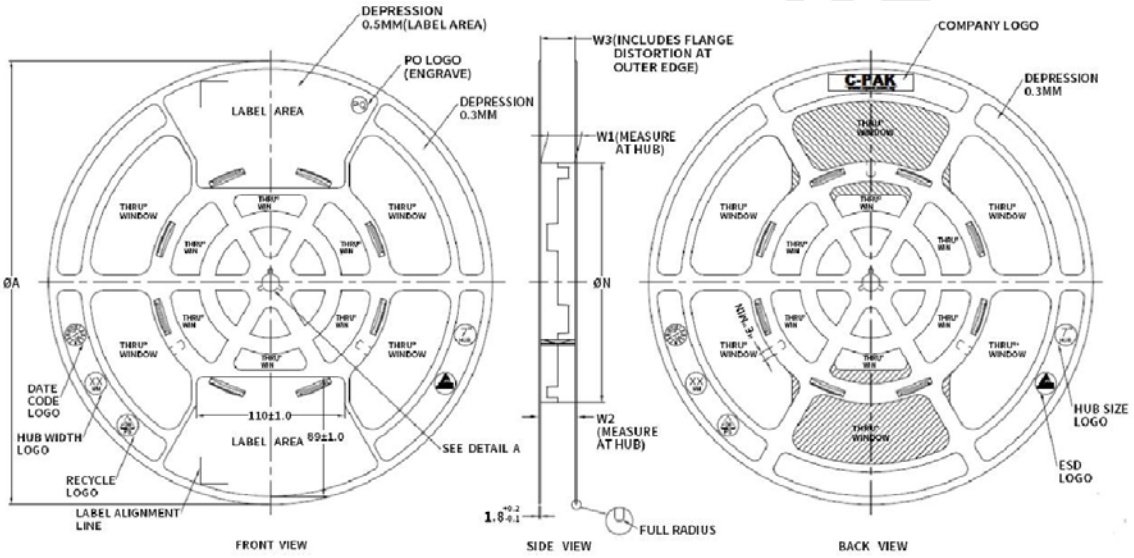
Figure 19. SOIC-16 Package Board Layout Example

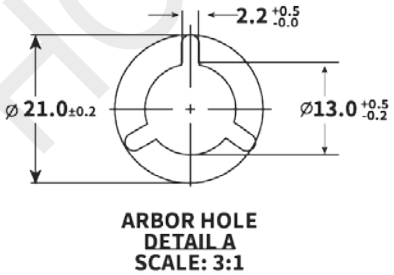
13 Ordering Information

Table 14. Part Number List

Part Number	MOQ	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	Package	MSL
CMT1050	1000	5	1	-40 to 125℃	SOW8L	3
CMT1042	1000	5	5	-40 to 125℃	SOW8L	3
CMT1050W	1000	5	1	-40 to 125℃	WB SOIC-16	3
CMT1052W	1000	5	5	-40 to 125℃	WB SOIC-16	3
CMT1042W	1000	5	5	-40 to 125℃	WB SOIC-16	3

14 Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 21. CMT10XXX Tape and Reel Information (for all packages)

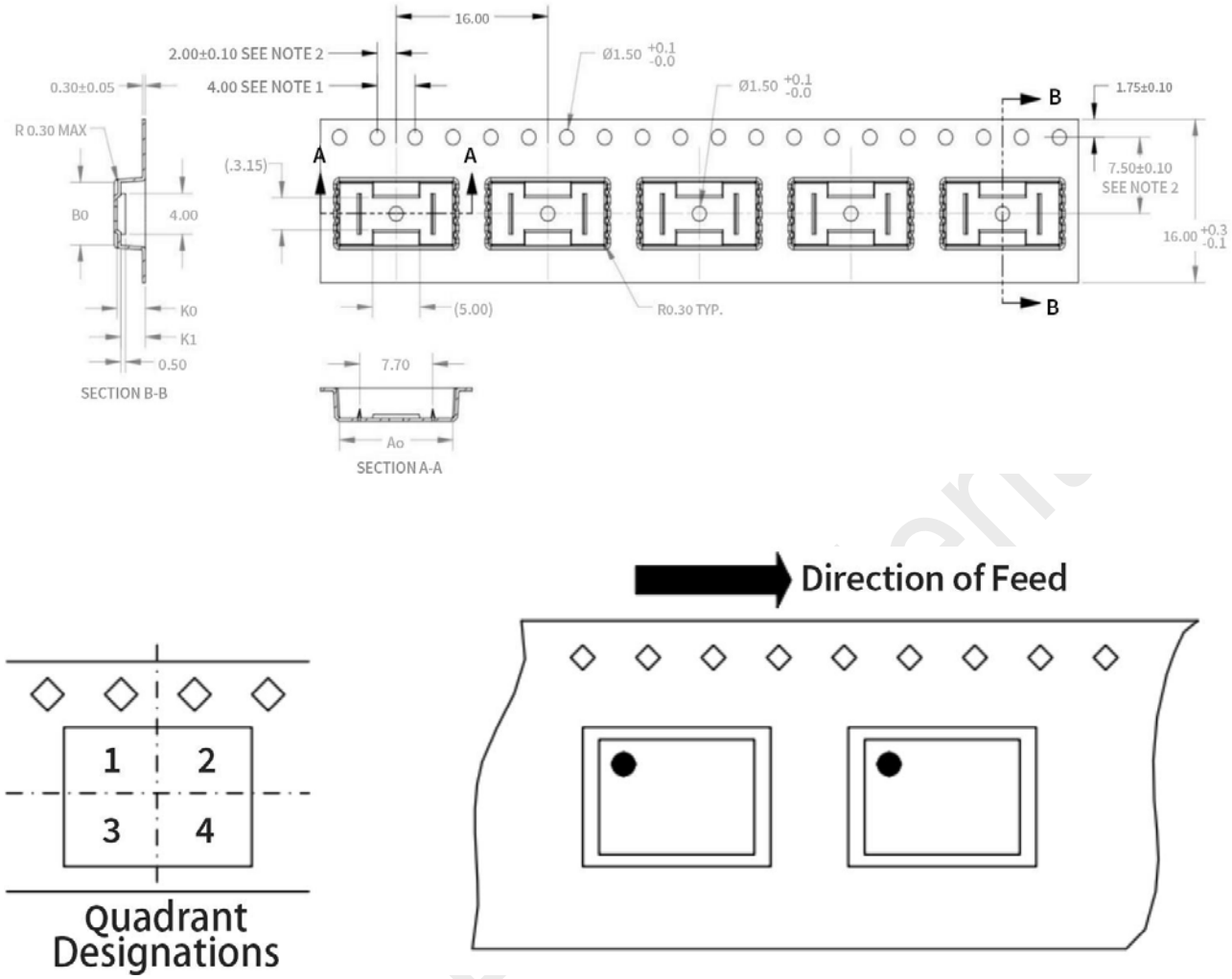
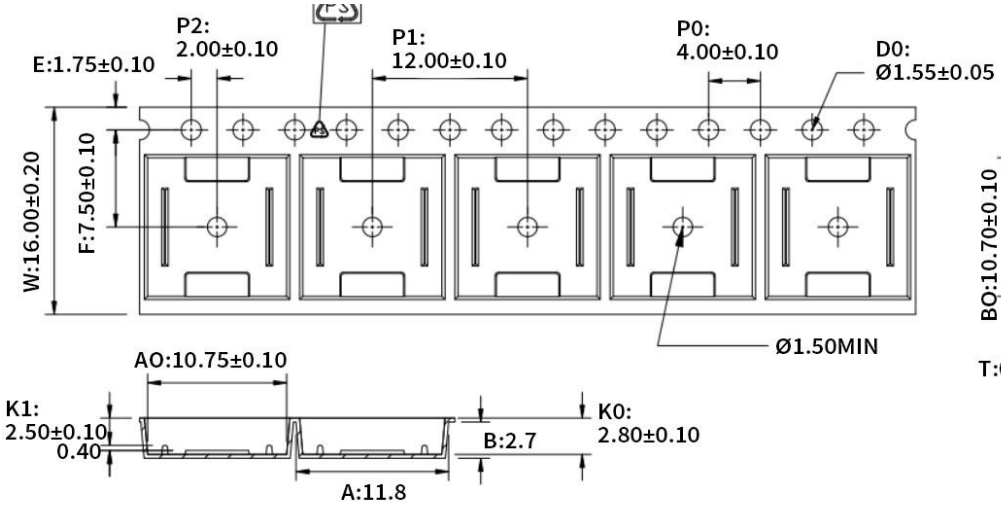


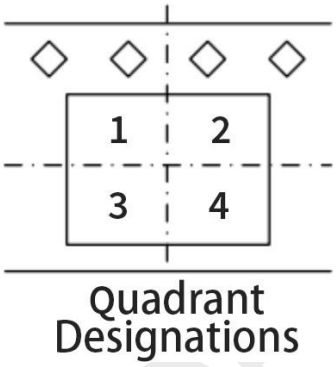
Figure 22. CMT10XXX SOIC8 Tape and Reel Information



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(復卷 N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ $10^{10}\Omega$/口

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



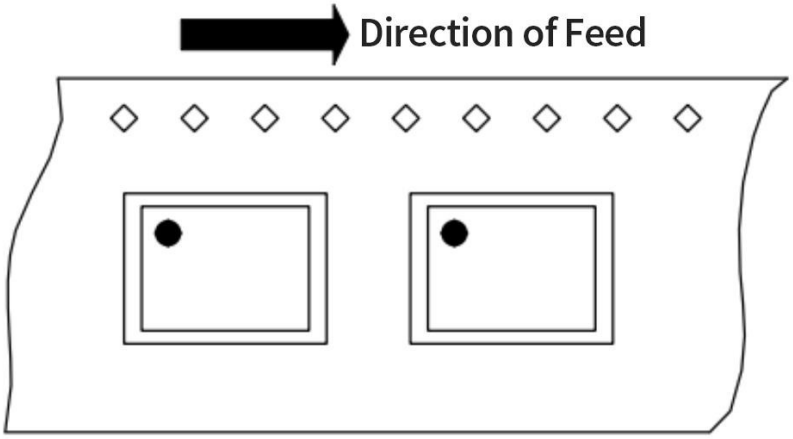


Figure 23. CMT10XXX SOIC 16 Tape and Reel Information

15 Appendix 1

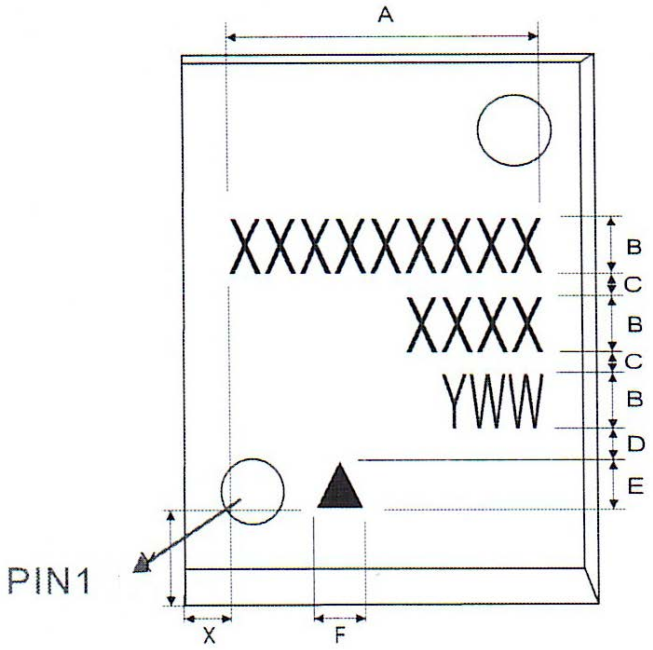


Figure 24. Silk Print Top View

16 Revise History

Table 14. Revise Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2023/09/26
0.2	8.2	Modified the typical application diagram	2023/11/14
0.3	All	Added data rate 1Mbps of CMT1050.	2024/6/17
	7	Update pin arrangement of CMT1042W	
	All	Update the UL certificate Number.	2024/10/30
		Add MSL level in order information	2024/12/3
0.4	All	Delete part number CMT1050U	2025/6/9
		Update the CQC certificate number	2025/7/3
0.5	12.2	Modify the package diagram of SOW16	2026/1/6
		Added Chapter 15, Appendix 1	
0.6	7	Revise the pin name and pin number of 6 and 7	2026/4/10

17 Contacts

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